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J. C. Patents, Inc.
4 Venture
Suite 250
Irvine, CA 92618

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/801,350
Filing Date: March 07, 2001
Appellant(s): LAI ET AL.

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Jiawei Huang
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 4/10/2006 appealing from the Office action mailed 4/27/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,982,601	Lin	11-1999
5,781,388	Quigley	7-1998
5,754,380	Ker et al.	5-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 3, 4 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Lin.

Lin teaches in figure 9 and related text an electrostatic discharge (ESD) protection circuit, suitable for use on the I/0 pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit (see figure 6 for clarity), which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad (Anode) and a ground voltage (Cathode), so as to discharge the electrostatic charges; and

an anti-latch-up circuit 51, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal A, respectively coupled to a

voltage source (the pad line), the ground voltage, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit A is directly connected to the third connection terminal of the SCR circuit, whereby an anti-latch-up voltage signal is sent from the sixth connection terminal to the SCR circuit, for preventing latching up of the SCR circuit during normal operation, wherein SCR circuit is triggered by an ESD event,.wherein a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation.

Regarding claim 3, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;

a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/0 pad 1; and a third N+ doped region, formed in the

N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line).

Regarding claim 4, Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

Claims 1, 3-4, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over by Quigley in view of Lin.

Regarding claims 1 and 13, Quigley teaches in figure 1 an electrostatic discharge (ESD) protection circuit, suitable for use on the I/0 pad, the ESD protection circuit comprising: a silicon controlled rectifier (SCR) circuit 22, which comprises a first connection terminal, a second connection terminal, and a third connection terminal, wherein the first connection terminal and the second connection terminal are respectively connected to the I/O pad and a ground voltage Vss, so as to discharge the electrostatic charges; and an anti-latch-up circuit RC 17, 18, which comprises a fourth connection terminal, a fifth connection terminal, and a sixth connection terminal 21, respectively coupled to a

voltage source (the pad line), the ground voltage Vss, and the third connection terminal of the SCR circuit, wherein the sixth connection terminal of the anti-latch-up circuit 21 is directly connected to the third connection terminal of the SCR circuit, wherein a voltage rising rate at a node of the anti-latch-up circuit can determine whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation. Although Quigley does not state a voltage source, this feature is inherent in Quigley's device as the line connected to the pad is the voltage source to the device. Furthermore, capacitor C also provides a voltage source to the device. Note that the device would not function without a voltage source.

Quigley does not explicitly state that the voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit.

Lin teaches in figures 6, 9 and 10 and related text a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a voltage rising rate at a node of the anti-latch-up circuit determines whether or not to trigger the SCR circuit for preventing latching up of the SCR circuit during normal operation in Quigley's device, in order to improve the protection capabilities of the device.

Regarding claims 3 and 4, Lin teaches in figure 5 an SCR circuit comprises: a P-type substrate; an N well, formed in the p-type substrate; a first P+ doped region, formed in

the P-type substrate and coupled to the ground voltage GND; a first N+ doped region, formed in the P-type substrate, adjacent to the first P+ doped region, and coupled to the ground voltage GND; a second N+ doped region, formed between the P-type substrate and the N well, adjacent to the first N+ doped region, and coupled via the third connection terminal of SCR circuit to the sixth connection terminal of the anti-latch-up circuit A, serving as a guard ring to collect electrons to avoid latch up when the anti-latch-up circuit sends signal through the sixth connection terminal to the third connection terminal of the SCR circuit during normal operation, and floating when the anti-latch-up circuit sends no signal to the SCR circuit during an ESD event;
a second P+ doped region, formed in the N well, adjacent to the second N+ doped region, and coupled to the I/0 pad 1; and a third N+ doped region, formed in the N well, adjacent to the second P+ doped region, and coupled to the voltage source (the pad line),

wherein Lin teaches in figure 6C an anti-latch-up circuit comprises: a capacitor C, having a first contact end and a second contact end, respectively coupled to the second N+ doped region and the ground voltage, and a resistor R, having a first end and a second end, respectively coupled to the voltage source and the second N+ doped region.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Quigley's device as taught by Lin, in order to improve the protection capabilities of the device.

Regarding claim 15, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse in Quigley's device in order to improve the protection capabilities of the device.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Quigley and Lin, as applied to claim 1 above, and further in view of Ker et al.

Quigley and Lin teach substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the 1/O pad

and a voltage source in the device of Quigley and Lin in order to provide better protection for the device against ESD event.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin.

Lin teach substantially the entire claimed structure, as applied to claim 1 above, including a RC delay time of the anti-latch-up circuit being greater than a voltage rising time of an ESD pulse.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit being smaller than a voltage rising time of an IC power in Lin's device in order to operate the device in its intended use.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin in view of Ker et al.

Lin teaches substantially the entire claimed structure, as applied to claim 1 above, except a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

Ker et al. teach in figure 1 a first diode 70, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode 60, having a first input end and a second input end, respectively connected to the I/O pad and a voltage source.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a first diode, having a first input end and a second input end, respectively connected to the ground voltage and the I/O pad; and a second diode, having a first input end and a second input end, respectively connected to the 1/O pad and a voltage source in Lin's device in order to provide better protection for the device against ESD event..

(10) Response to Argument

1. Appellant argues on pages 8 and 9 that "Lin substantially fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/0 pad and the fourth connection terminal of the transient circuit is connected to the voltage source. Instead Lin substantially teaches or discloses that the connection terminals of BOTH transient oscillator circuit 61 and SCR circuit are connected to the same VDD bus or the same I/0 PAD". Appellant further argues that "the language "the first connection terminal (112, of the SCR circuit) is connected to a I/0 pad" and "the fourth connection terminal (126) of the anti-latch-up circuit) is coupled to a voltage source

(Vcc)" clearly indicate that the I/O PAD and the VOLTAGE SOURCE are TWO SEPARATE ELEMENTS", as depicted in figure 4.

Claim 1 recites a first connection terminal of the SCR circuit is connected to an I/0 pad and a fourth connection terminal of an anti-latch-up circuit is coupled to the voltage source.

Appellant teaches in figure 4 a first connection terminal 112 of the SCR circuit is connected to an I/0 pad 100, and a fourth connection terminal 126 of the anti-latch-up circuit is coupled to a voltage source Vcc. Figure 4 further depicts that the first connection terminal 112 and the fourth connection terminal 126 are connected to each other via diode 108. These connections are also depicted in figure 5, wherein the first connection terminal of the SCR circuit (the circuit comprising the two transistors and two resistors) is connected to an I/0 pad, and a fourth connection terminal of the anti-latch-up circuit (the RC circuit) is coupled to a voltage source Vcc. That is, both terminals are connected to one common horizontal line, which branches out to the I/0 pad and the voltage source. This circuit/drawing is identical to the circuit depicted in figure 6A of Lin (with the exception of appellant's diode 108 which is connected between the I/0 pad and the voltage source), wherein the first connection terminal line and the fourth connection terminal are also connected to one common horizontal line which branches out to the I/0 pad (PAD) and the voltage source Vh.

Clearly, Lin does not teach that the I/0 pad, the voltage source Vh and the voltage bus Vdd are all the same element. The fact that the first connection terminal

line and the fourth connection terminal line of Lin (and of appellant) are connected to one common horizontal line which branches out to the I/0 pad and the voltage source, does not mean that the I/0 pad and the voltage source are the same element.

Furthermore, Lin teaches "a first connection terminal of the SCR circuit is connected to an I/0 pad and a fourth connection terminal of an anti-latch-up circuit is coupled to the voltage source", as recited in claim 1, because Lin teaches in figure 6A a first connection terminal of the SCR circuit (the vertical line located adjacent to "P+ region") is connected to an I/0 pad (via the horizontal line) and a fourth connection terminal of an anti-latch-up circuit (the vertical line located above "transient oscillator 61") is coupled to the voltage source Vh. Please note that the device would not operate without a voltage source.

2. Appellant argues on pages 12 and 13 that Quiley, as Lin above, fails to teach or disclose that the first connection terminal of the SCR circuit is connected to the I/0 pad and the fourth connection terminal of the transient circuit is coupled to the voltage source, because the first connection terminal and the fourth connection terminal are connected to the same I/0 pad.

As discussed above, both appellant and Lin teach a first connection terminal line and a fourth connection terminal line being connected to one common horizontal line which branches out to an I/0 pad and a voltage source. Quigley also teaches in figure 1 a first connection terminal line and a fourth connection terminal line being connected to

one common horizontal line, which branches out to an I/0 pad and a voltage source, for the following reasons:

It is clear from figure 1 that Quigley teaches a first connection terminal of the SCR circuit 22 being connected to an I/0 pad. Quigley further teaches a fourth connection terminal of an anti-latch-up circuit RC 17, 18 being coupled to the common horizontal line. The common horizontal line is coupled to a voltage source, for the following reasons: A device would not function without a voltage source and a ground connection. Therefore, although figure 1 of Quigley does not depict both the voltage source and the ground connection, these connections must be inherent in Quigley's device. That is, a voltage drop must be present between the "Vss" node and the horizontal line connected to the pad. Furthermore, Quigley teaches that the RC circuit 17, 18 is a voltage divider. That is, a voltage must exist across the RC circuit, i.e. between the "Vss" node and the horizontal line connected to the pad. This voltage can also be considered as a voltage source to the device. Thus, since a voltage to operate the device must be present at the horizontal line, then Quigley teaches a fourth connection terminal of an anti-latch-up circuit RC 17, 18 being coupled to a voltage source, as claimed.

3. Appellant argues on pages 13-15 that Quigley and Lin do not teach a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as recited in claim 15, because the mechanism of preventing triggering and triggering of the SCR circuit of the claimed

invention is substantially different from that of Quigley who sets the threshold voltage for triggering the SCR circuit and prolongs the delay time of the SCR circuit to prevent normal signals from triggering the SCR circuit. Appellant further argues that Quigley teaches away from the claimed invention, and an artisan would not be motivated to modify the ESD circuit of Quigley.

Although Quigley sets the threshold voltage for triggering the SCR circuit and prolongs the delay time of the SCR circuit to prevent normal signals from triggering the SCR circuit, Lin provides an advantageous reasons to further modify and fine tuning the parameters of the capacitor and the resistor of the RC circuit so that the SCR is easier to be triggered during an ESD event, and that the SCR does not trigger during normal operation or powering up.

Lin explicitly teaches that using an RC relay time of the RC anti-latch-up circuit larger than the voltage rising phase of the ESD transient, would more easily trigger the SCR during an ESD event (column 4, lines 26-32). Lin further teaches that using an RC relay time of the RC anti-latch-up circuit less (smaller) than the powering up transient, would prevent the SCR from being triggered during normal operation or powering up. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power and greater than a voltage rising time of an ESD pulse, as taught by Lin, in Quigley, as claimed.

4. Appellant argues on page 18 that Lin does not teach a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power but greater than a voltage rising time of an ESD pulse, as recited in claim 15, because Lin states in column 3, lines 48-53 that "the voltage transition provided by the voltage transition circuit (51) has a ramp rate faster than the ESD voltage's ramp rate", and this means that Lin teaches "RC delay time smaller than the ESD voltage ramp rate".

Lin's statement that "the voltage transition provided by the voltage transition circuit (51) has a ramp rate faster than the ESD voltage's ramp rate", does not mean that Lin teaches "RC delay time smaller than the ESD voltage ramp rate". In fact, Lin teaches in column 4, lines 26-32 that "The time constant of R1C1 is preferably larger than the voltage rising phase of the ESD transient, for example, R1C1>50 ns, such that the SCR is easy to trigger during an ESD event. R1C1 is also preferably less than the powering up transient, for example R1C1<1 micros, such that the SCR, does not trigger during normal operation or powering up." An artisan reading this statement would be motivated to use an RC relay time of the RC anti-latch-up circuit larger than the voltage rising phase of the ESD transient, so that the SCR is easy to trigger during an ESD event. An artisan would also be motivated to use an RC relay time of the RC anti-latch-up circuit less (smaller) than the powering up transient, so that the SCR does not trigger during normal operation or powering up. Therefore, it would be have been obvious to an artisan to use a RC delay time of the anti-latch-up circuit is smaller than a voltage rising time of an IC power and greater than a voltage rising time of an ESD pulse in Lin's device, as claimed.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Ori Nadav

Conferees:

Drew Dunn

Lynne Gurley

Ori Nadav